

ColorBoard 264 (Cheapskate) Specification

July 28, 1988

Primary Design Goal

Replacement for ColorBoard 64 and 64N, with features to support Apple's Full Color QuickDraw, and optional NTSC output via a daughterboard. Once 264 production starts, 64 and 64N production stops.

Target Retail Price

\$1595

Availability

Introduction	November 1988
Shipping	January 1989

Resolution

640x480	66Hz	13" monitor	72 DPI
640x486	30Hz	NTSC	

One local oscillator with one external (NTSC). Resolutions are software selectable (no DIP switches), via keyboard at boot time.

1.5 Meg video RAM (1024 x 512 x 24 bits)

Pixel Depth

1,2,4,8 and 24 bits per pixel. 1,2,4, and 8 bits per pixel is indexed; 24 bits per pixel is full chunky direct. 24-bit chunky planar hardware available; availability in software with release 1.0 TBD.

Chunky planar available in hardware, availability with release 1.0 ROM TBD.

Max 256 colors (indexed) and 16.7 million colors (direct) from 16.7 million palette.

Configuration ROM

27256 EPROM (32K bytes)

Video

- RS-343A compatible
- 15 pin D-subminiature connectors (same as Apple's)
- 35Khz monitors supported (optional 31.49Khz)
- VLSI controller
- NTSC output (optional)
- Separate sync for VGA compatability

Slot

- Single NuBus slot
- 32-bit addressing (fat slot)
- X Amps at 5 Volts
- NTSC option control bus

Register	Add 15.0	Bits	Default Value	Description
CMODE	6004	3RW	1** CHUNKY MODE	CHUNKY , MODE1 , MODE0
CMODE	6008	3C	000 1 BIT MODE	CHUNKY , MODE1 , MODE0
			001 2 BIT MODE	
			010 4 BIT MODE	
			011 8 BIT MODE	
OSC30HZ	600C	2RW	00	OSCSEL , 30 HZ MODE
NMRQ	6010	1RW	0	NMRQ BIT
NMRQ	6014	1C	N/A	NMRQ BIT
DACCTL	6018	2RW	00 CHUNKY	DACS1 , DACS0
			10 PSEUDO COLOR	
FORCEBLK*	601C	1RW	1	FORCE BLANK (ACTIVE LOW)
EXSYNMODE	6020	1RW	0	ENABLES EXTERNAL SYNCs
FATSLOT	6024	1RW	1 FAT SLOT	FORCES FAT SLOT ADD DECODE
			0 SKINNY SLOT	
RDOUTST	6028	1R	N/A	READS MPRES , MTYPE , OPTON
SYNCEN	602C	1RW	1	ALLOWS SYNC TO GO ACTIVE
TRANSEN	6030	1RW	1	TRANSFER CYCLE ENABLE
STVTOTAL	6034	1R	N/A	READS VTOTAL FROM VIDEO
VCNTRES	6038	1RW	0	RESETS ALL VIDEO COUNTERS
NMRQDIS	603C	1RW	0	DISABLE THE NMRQ INTERRUPT
VSYNEND	6040	4RW	002 HEX	VERTICAL SYNC END COUNT
VBLKGO	6044	10RW	209 HEX	VERTICAL BLANK START COUNT
VTOTAL	6048	10RW	20C HEX	VERTICAL TOTAL COUNT
HSYNCEND	604C	9RW	00F HEX	HORIZONTAL SYNC END COUNT
HBLKEND	6050	9RW	027 HEX	HORIZONTAL BLANK END COUNT
HBLKGO	6054	9RW	0C7 HEX	HORIZONTAL BLANK START COUNT
HTOTAL	6058	9RW	0D7 HEX	HORIZONTAL TOTAL COUNT
HHLFLIN	605C	9RW	06B HEX	HORIZONTAL HALFLINE COUNT
VBLKEND	6060	6RW	029 HEX	VERTICAL BLANK END COUNT
BLKENABLE	6064	1RW	0	THIS BIT ENABLES BLOCK MODE

Bits Definition

R - Readable

W - writeable

C - Clearable

Clearing a register is done by writing to the registers clear address with a 1 in each bit position to be cleared.

* DO NOT CARE

CHEAPSKATE BOARD ADDRESS SPACE (FAT SLOT)

COMPONENTS	ADDRESS SPACE NEEDED IN HEX	
RAM	20 0000	2M BYTES
STATUS	0 1000	4K BYTES
DAC CONTROL	0 1000	4K BYTES
ROM	0 8000	32K BYTES

ROM ADDRESS LINES ARE AD<14..2>

~~SKINNY SLOT~~

FsFF FFFF

ROM 32K BYTES

FsFF 8000

FsFF 7FFF

DAC 4K BYTES

FsFF 7000

FsFF 6FFF

STATUS REGISTERS 4K

FsFF 6000

FsFF 5FFF

UNUSED ILLEGAL ADDRESSES

Fs20 0000

Fs1F FFFF

RAM 2M BYTE

Fs00 0000

* DO NOT CARE

~~F55xxxxx
 24 F50xxxxx
 32 F55xxxxx~~

CHEAPSKATE BOARD ADDRESS SPACE (SKINNY SLOT)

COMPONENTS	ADDRESS SPACE NEEDED IN HEX	
RAM	8 0000	524K BYTES
STATUS	0 1000	4K BYTES
DAC CONTROL	0 1000	4K BYTES
ROM	0 8000	32K BYTES

ROM ADDRESS LINES ARE AD<14..2>

SKINNY SLOT

Fs*F FFFF

ROM 32K BYTES

Fs*F 8000

Fs*F 7FFF

DAC 4K BYTES

Fs*F 7000

Fs*F 6FFF

STATUS REGISTERS 4K

Fs*F 6000

Fs*F 5FFF

UNUSED ILLEGAL ADDRESSES

Fs*8 0000

Fs*7 FFFF

RAM .5M BYTE

Fs*0 0000

* DO NOT CARE

COLORBOARD 264

Specification

Revision C1

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RasterOps Corporation

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CONFIDENTIAL

1.0 Introduction

This document establishes the physical and electrical characteristics for the ColorBoard 264 System. ColorBoard 264, referred to as 264 throughout the rest of this document, is a medium resolution, high speed, graphics display system for the Macintosh II, IIX, and IICX. The 264 occupies 1 Nubus slot. It is capable of five pixel depths and two resolutions. A block diagram of the 264 is shown in figure 1-1. This document is the property of RasterOps Corporation and is confidential. Reproduction of this document is prohibited.

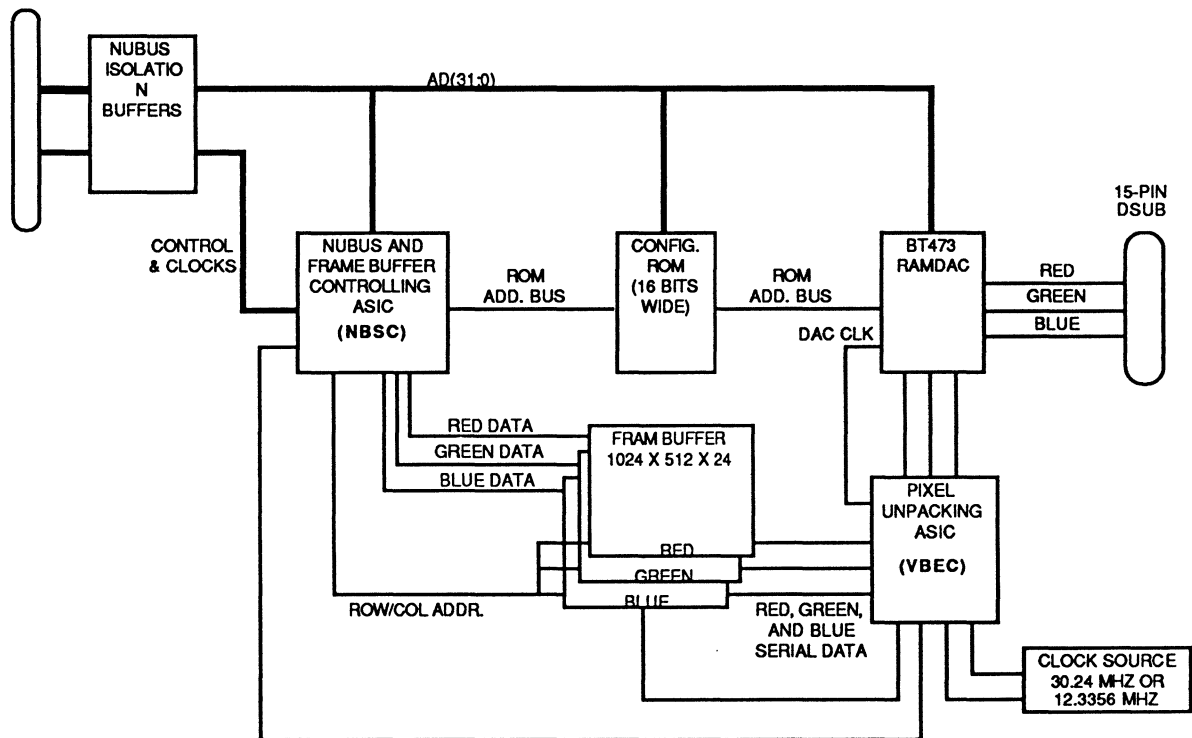


Figure 1-1 264 Block Diagram

2.0 Hardware Description

2.1 Features

Switchable Resolutions of

- 640 x 480
- 640 x 480 x 30Hz (NTSC Frequencies)

Pixel Depths of 1, 2, 4, 8, 24-Bits

- 24-Bit Mode is Full Chunky

Macintosh II "FAT" and "Skinny" NuBus Compatible

16.7 Million Color Palettes

30.24 and 12.3356 MHz Video Rate

Single NuBus Slot

Current Consumption of 1.40 Amps at 5 Volts

300 nS Cycle for 24-Bit Pixels

RS-343 Compatible

15-Pin D-Subminiature Connector (Same as Apple)

State of the Art Surface Mount Technology Including two ASICs

Supports Nubus Block Mode

2.2 Overview

The 264's function is to provide a inexpensive 24-bit solution for the Macintosh user. The 264 supports all pixel depths the user could ever need, from 1-Bit for speedy drawing all the way up to 24-Bit for true color reproduction. Added feature include full support of block mode transfers over the Nubus [™] and NTSC frequency compatibility.

3.0 Technical Data

3.1. Absolute Maximum Ratings

Supply Voltage, VCC	5.25 Volts
Operating Ambient Temperature Range	0 °C to 60 °C
Storage Temperature	-65 °C to 150 °C
ICC (Supply Current)	1.5 A @ 5.25 V

3.2 Reference Drawings

The following items should be referenced for detailed information on the 264 system.

264 Top Assembly LM.....	264
264 Top Assembly Drawing	0002-0066
264 Assembly Drawing	0002-0063
264 Schematics	0002-0062
264 PCB Fab	0002-0064
264 L/M	0002-0065

3.3 Video Specifications

3.3.1 Resolution 640 x 480 67 Hz

1 Pixel = 33.06878 nS = 30.24 MHz
 1 VidClk = 529.1005 nS = 1.89 MHz
 640 Pixels Horizontal Visible
 864 Pixels Horizontal Total
 64 Pixels Horizontal Front Porch
 64 Pixels Horizontal Sync
 96 Pixels Horizontal Back Porch
 480 Lines Vertical Visible
 525 Lines Vertical Total
 3 Lines Vertical Front Porch
 3 Lines Vertical Sync
 39 Lines Vertical Back Porch
 Horizontal Frequency = 35.0000 KHz
 Vertical Frequency = 66.6666 Hz

3.3.2 Resolution 640 X 480 30 Hz NTSC

1 Pixel = 81.0662 nS = 12.3356 MHz
1 VidClk = 324.265 nS = 3.0839 MHz
640 Pixels Horizontal Visible
784 Pixels Horizontal Total
12 Pixels Horizontal Front Porch
84 Pixels Horizontal Sync
48 Pixel Horizontal Back Porch
480 Lines Vertical Visible
525 Lines Vertical Total
3 Lines Vertical Front Porch
3 Lines Vertical Sync
17 Lines Vertical Back Porch
Horizontal Frequency = 15.733 KHz
Vertical Frequency = 30.00 Hz

4.0 Addressing

The 264 needs almost 2.5 MBytes of addressable space to run in 24-Bit mode. As a result, to use 24-Bits per pixel, the Macintosh II must be capable of running Apple's 32-Bit QuickDraw and it must be installed. The 264 will also run under Apple's 8-Bit QuickDraw but 24 bit mode is not a selectable pixel depth in the Control Panel. The 16 Megabyte memory map is provided in Figure 4-1 and the Subaddress map for Registers, DAC etc. is shown in Figure 4-2.

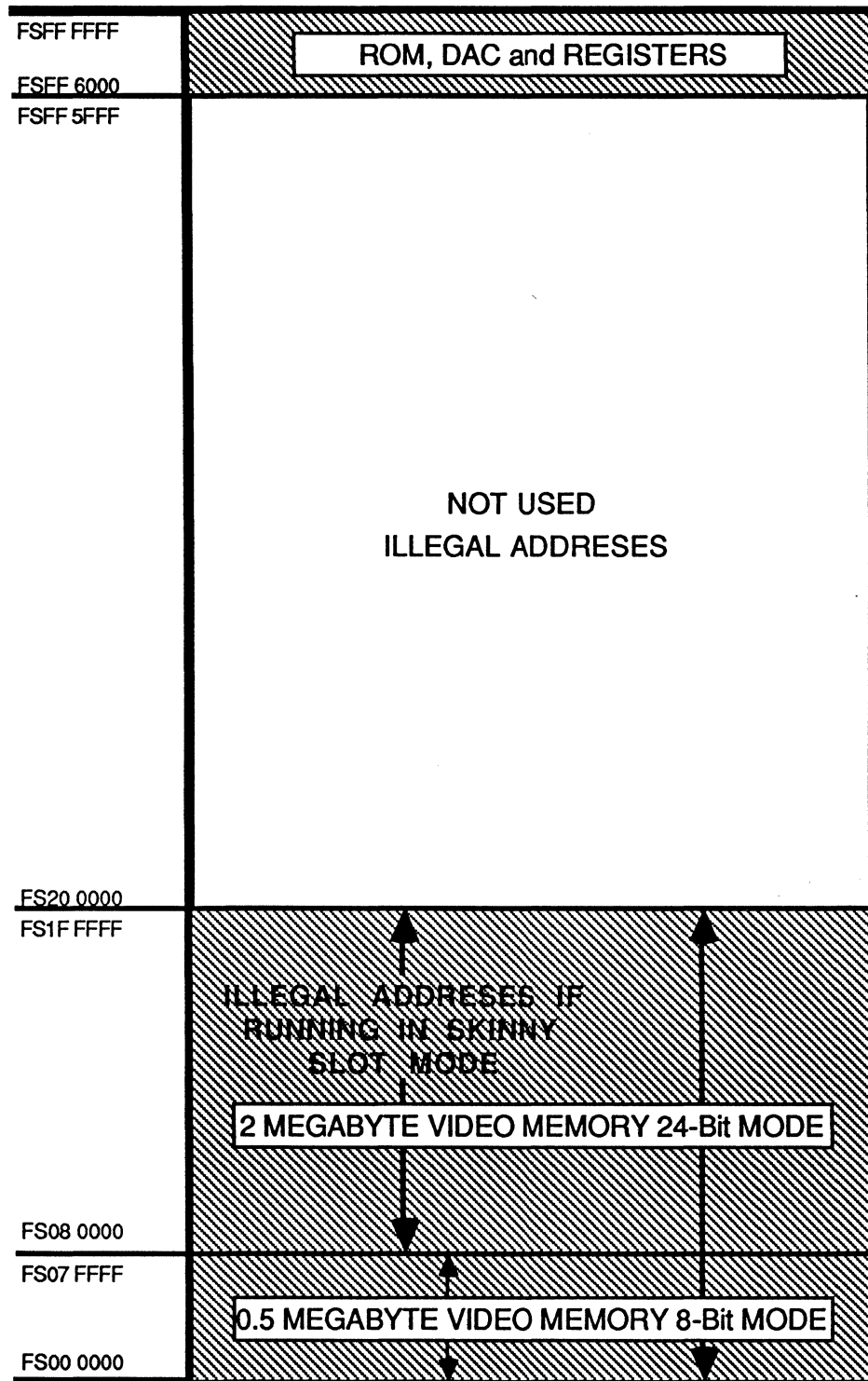


Figure 4-1 16 Megabyte Memory Map

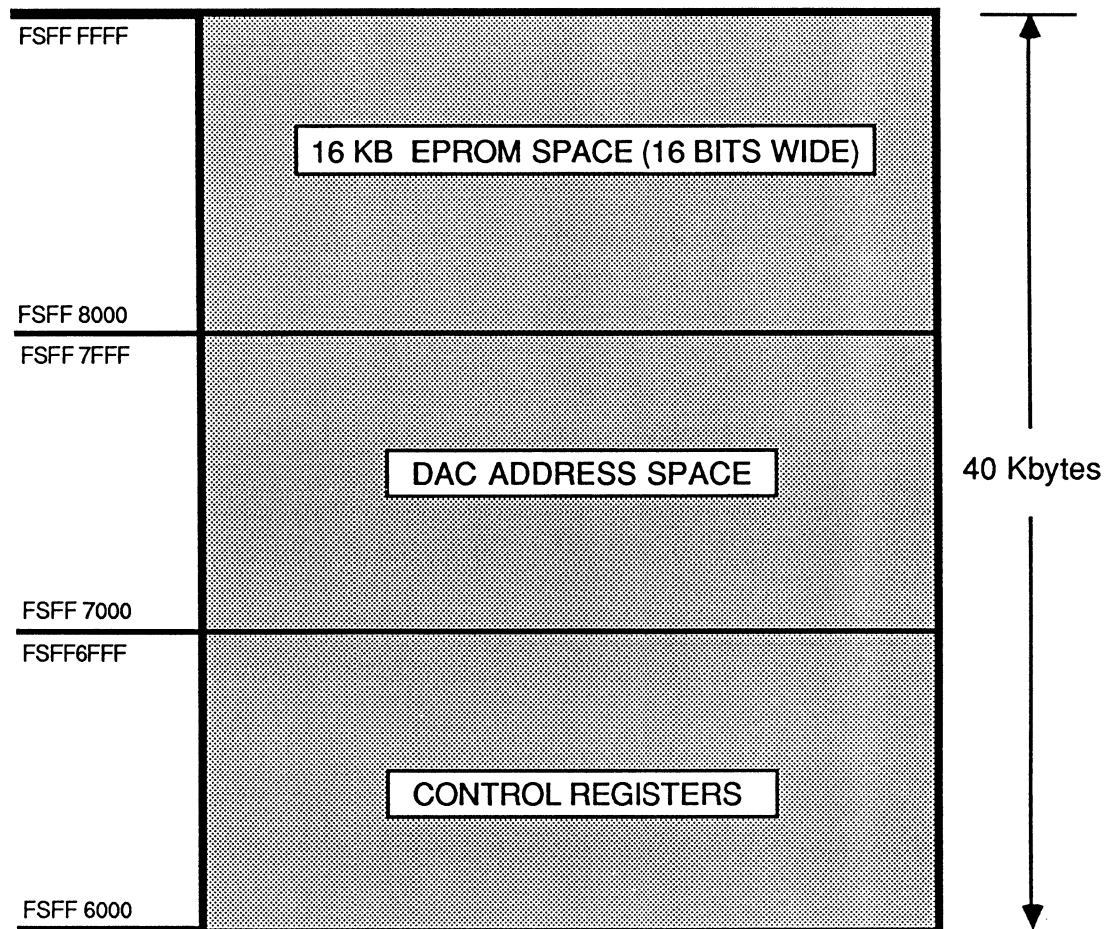


Figure 4-2 Subaddress Map

4.2 Nubus System Controller ASIC (NBSC CHIP)

4.2.1 Introduction

In order to facilitate performance and reduce cost as much as possible, the entire nubus, frame buffer, and video timing control logic was integrated into a single Toshiba ASIC (Application Specific Integrated Circuit). This ASIC is approximately 10,000 gates, uses a three phase clock (delayed versions of the 10 MHz Nubus clock) and is implemented in a 1.5 μ M technology. There are several internal registers which control how the part will behave such as decode modes and video timing. The following sections explain the chip in a more detail and what the internal register addresses and functions are.

4.2.2 A look at the NBSC chip

The NBSC chip is a NUBUS responder. It receives buffered versions of all necessary NUBUS lines and does a fixed address decode depending on whether the chip is being addressed in fat slot mode or skinny slot mode.

The NBSC chip NUBUS interface has two primary operating modes , chunky mode and nonchunky mode. In nonchunky mode NBSC chip supports all NUBUS transactions including Block mode operations, which are not currently supported on the Mac II. In chunky mode, only longword transactions and block mode transactions are supported.

The video RAM address, data and control lines are driven directly by the NBSC chip. Conceptually the VRAMs are divided into three banks, Red, Green and Blue. When operating in nonchunky mode only the Red bank of RAMs is active. This provides a 16 bit interface so page mode access is used to transfer 32 bits. This corresponds to 1, 2, 4, or 8 bit modes for the VBEC. In Chunky mode, 24 bit mode, all three banks of RAMs are driven and each 32 bit quantity transfers 8 bits of data to each bank.

When the NBSC chip detects an access to the ROM address space, the appropriate address bits are latched and the ROM chip enable and output enable are asserted. This interface provides capability for connecting from one to four (two in the case of the 264) 8Kx8 ROMs. One ROM may be connected to each byte lane of the NUBUS.

The NBSC chip provides the interface to the DACs CLUT and control registers. It is designed to work with the BT473 or BT478. The ROM address lines are also latched for a DAC access, which provides the DAC address bits RS[2:0].

The NBSC chip also provides registers to control the operating mode of the VBEC. The NBSC chip contains a programmable video timing generator. The video timing circuit generates composite sync, composite blank and controls the transfer and refresh cycles. It is also capable of operating from an external sync source. Video timing signals generated in the NBSC chip are then sent to the VBEC chip. The VBEC controls the serial port from the VRAMs to provide data in sync with the DAC control signals.

The Video RAM interface does three basic operations, a read cycle, a write cycle, and a transfer/refresh cycle. For block mode transactions, the last period of the read and write cycle are repeated as

necessary to complete the cycle. In chunky mode, one longword is transferred each cycle, while in nonchunky mode, each longword takes two cycles to transfer. The VRAMs are grouped into three banks, Red, Green and Blue. In non chunky mode only the Red bank of VRAMs is used and bits are packed according to Apples standard. In 24-bit mode the pixels are also packed according to Apple's video standard and the zero filling is provided by NBSC chip. The lines to the VRAMs correspond one to one with the data and control lines needed by the VRAMs. The only exception is the to CAS lines, -CASH and -CASL. In nonchunky mode , the Red bank acts as a 16 bit port. In chunky mode all three banks act as 8 bit ports. This is accomplished by using two separate CAS lines. In nonchunky mode both -CASH and -CASL are active at the same time, while in chunky mode only one or the other is active.

The transfer/refresh cycle is initiated when the Horizontal counter is equal the Horizontal total register. Since this request comes off of a Video clock the request is internally synchronized to Nubus Clock then arbitrated for. The arbitration scheme simply guarantees that once a request is issued and synchronized, it will run immediately, or after the currently executing NUBUS request completes. In case of a tie, the NUBUS request will run first. If a NUBUS request comes in while the transfer/refresh cycle is active it will be stalled until the transfer/refresh cycle completes. A transfer/refresh cycle consists of a transfer cycle followed by four CAS before RAS refresh cycles.

4.2.3 System Control Registers

NAME: CMODE

ADDRESS: FSFF 6004 (FSFF 6008 FOR MASKED CLEAR)

ACCESS: READ/WRITE, CLEAR (AT PROPER ADDR.)

DEFAULT VALUE: 07 (HEX)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
X	X	X	X	X	CHUNKY	MODE1	MODE0

1, 2, 4, 8 BIT MODE	0	X	X
CHUNKY (24 BIT) MODE	1	X	X
SELECT 1 BIT UNPACKING	X	0	0
SELECT 2 BIT UNPACKING	X	0	1
SELECT 4 BIT UNPACKING	X	1	0
SELECT 8 BIT UNPACKING	X	1	1

This register is used to control the mode of operation for the Video Back End Chip (VBEC). These signals correspond to the NBSC Chip pins of the same name. The value of this register may be changed at any time but the value of the corresponding pin will only change at the beginning of composite sync. It is important to note that if the Chunky bit is set to logic 1, the hardware guarantees that the Mode1 and Mode0 outputs will be set to a logic 1 regardless of the state of the register bits.

NAME: OSC30HZ

ADDRESS: FSFF 600C

ACCESS: READ/WRITE

DEFAULT VALUE: 00 (HEX)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
X	X	X	X	X	X	OSCSEL	+30 HZ MODE

SELECT 30.24 MHZ OSC.	0	X
SELECT 12.3356 MHZ OSC.	1	X
SELECT 60 HZ INTERLACED MODE	X	0
SELECT 30 HZ NON-INTERLACED MODE	X	1

This register has two unrelated control bits. OscSel is actually a general purpose status register bit which drives an output on the NBSC Chip. In the 264 implementation, this bit is used to control the oscillator select input on the VBEC chip.

The NBSC Chip video timing generator is capable of producing NTSC video signals. NTSC mode, also referred to as 30Hz mode, is selected by this status register bit.

NAME: NMRQ

ADDRESS: FSFF 6010 (FSFF 6014 FOR CLEAR)

ACCESS: READ/WRITE, CLEAR (AT PROPER ADDR.)

DEFAULT VALUE: 00 (HEX)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
X	X	X	X	X	X	X	+NMRQ

NO INTERRUPT 0

INTERRUPT PENDING 1

This bit is the drives the NMRQ interrupt line to the Nubus. After reset, this bit is disabled until this register is written to any value. At that point it is enabled and will be set whenever vertical count is zero. This interrupt may be disabled by writing to the NMRQDIS register.

NAME: DACCTL

ADDRESS: FSFF 6018

ACCESS: READ/WRITE

DEFAULT VALUE: 00 (HEX)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
X	X	X	X	X	X	DACS1	DACS0

24 BIT FULL CHUNKY	0	0
8 BIT PSEUDO COLOR	1	0
NOT SUPPORTED	1	1
NOT SUPPORTED	0	1

This register is a general purpose status register whose bits drive output pins on the NBSC Chip. In the 264 implementation, these bits are used to drive the S1 and S0 bits (mode select inputs) of the BT473 (Digital to Analog Converter).

NAME: FORCEBLK

ADDRESS: FSFF 601C

ACCESS: READ/WRITE

DEFAULT VALUE: 01 (HEX)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
X	X	X	X	X	X	X	-FORCE BLANK

SCREEN BLANKED	0
SCREEN UNBLANKED	1

When this register is a logic zero it forces the composite blank output to be in the active state.

NAME: FATSLOT

ADDRESS: FSFF 6024

ACCESS: READ/WRITE

DEFAULT VALUE: 01 (HEX)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
X	X	X	X	X	X	X	+FAT SLOT

USE SKINNY SLOT DECODES 0

USE FAT SLOT DECODES 1

This bit when set causes the chip to decode addresses produced by using 32-bit mode of the Macintosh (Fat Slot). When this bit is a logic 0 the chip decodes addresses produced using 24-bit mode of the Macintosh (Skinny Slot).

NAME: RDOUTST

ADDRESS: FSFF 6028

ACCESS: READ ONLY

DEFAULT VALUE: N/A

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
X	X	X	X	X	+MONIT. PRESNT	MONIT. TYPE	-OPTION

MONITOR NOT CONNECTED 0 X X

MONITOR CONNECTED 1 X X

60 HZ NON-INTERLACED X 0 X

30 HZ INTERLACED X 1 X

OPTION RAM CONNECTED X X 0

OPTIONAL RAM NOT CONNECTED X X 1

This register provides general purpose register inputs from the NBSC Chip pins of the same name. These inputs are synchronized to the Nubus clock and are then available to be read.

NAME: NMRQDIS

ADDRESS: FSFF 603C

ACCESS: READ/WRITE

DEFAULT VALUE: 00 (HEX)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
X	X	X	X	X	X	X	+NMRQ DIS.

NMRQ ENABLED 0

NMRQ DISABLED 1

This register is provided so software can disable the NMRQ interrupt output. While this bit is a logic 1, the NMRQ interrupt is disabled.

NAME: BLKENABLE

ADDRESS: FSFF 6064

ACCESS: READ/WRITE

DEFAULT VALUE: 00 (HEX)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
X	X	X	X	X	X	X	+BLKEN

BLOCK MODE DISABLED 0

BLOCK MODE ENABLED 1

This bit exists for IC Tester requirements and should be set at initialization and left.

4.2.4 Video Control Registers

NAME: FORCEBLK

ADDRESS: FSFF 601C

ACCESS: READ/WRITE

DEFAULT VALUE: 01 (HEX)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
X	X	X	X	X	X	X	-FORCE BLANK

SCREEN BLANKED 0
 SCREEN UNBLANKED 1

Using this register the screen can be forced to be blank.

NAME: EXSYNMODE

ADDRESS: FSFF 6020

ACCESS: READ/WRITE

DEFAULT VALUE: 00 (HEX)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
X	X	X	X	X	X	X	+EN EXSYN

USE INTERNAL SYNCs 0
 USE EXTERNAL SYNCs 1

When this bit is a logic one it puts the CHBUS chip in external sync mode.

NAME: SYNCEN

ADDRESS: FSFF 602C

ACCESS: READ/WRITE

DEFAULT VALUE: 01 (HEX)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
X	X	X	X	X	X	X	+SYNC EN

SYNCS DISABLED 0

SYNCS ENABLED 1

When set, this bit allows the video timing generator to produce composite sync. When this bit is a logic zero, the composite sync output is forced to its unasserted state.

NAME: TRANSEN

ADDRESS: FSFF 6030

ACCESS: READ/WRITE

DEFAULT VALUE: 01 (HEX)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
X	X	X	X	X	X	X	+TRANS EN

TRANSFER CYCLES DISABLED 0

TRANSFER CYCLES ENABLED 1

When set this bit enables transfer cycles and refresh cycles. Refresh cycles occur immediately after transfer cycles. Four refresh cycles occur after every transfer cycle. Transfer cycles are initiated by the Horizontal count being equal to zero.

NAME: STVTOTAL

ADDRESS: FSFF 6034

ACCESS: READ ONLY

DEFAULT VALUE: N/A

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
X	X	X	X	X	X	X	STVTOT

VTOTAL $\neq$ VCOUNT 0

VTOTAL = VCOUNT 1

This bit enables software to read the VTtotal bit from the video timing generator. This bit is a logic 1 when VTtotal = VCount.

NAME: VCNTRES

ADDRESS: FSFF 6038

ACCESS: READ/WRITE

DEFAULT VALUE: 00 (HEX)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
X	X	X	X	X	X	X	+CNTR RESET

COUNT ENABLED 0

COUNTERS RESET 1

When set, this bit resets all video counters and holds them at logic zero.

4.2.5 Video Timing Registers

NAME: VSYNEND

ADDRESS: FSFF 6040

ACCESS: READ/WRITE

DEFAULT VALUE: 02 (HEX)

BIT 9	BIT 8	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
X	X	X	X	X	X	VSE3	VSE2	VSE1	VSE0

This register sets the Vertical Sync End count. It should be equal to the number of VIDCLKS in the sync period minus one.

NAME: VBLKEND

ADDRESS: FSFF 6060

ACCESS: READ/WRITE

DEFAULT VALUE: 029 (HEX)

BIT 9	BIT 8	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
X	X	X	X	VBE5	VBE4	VBE3	VBE2	VBE1	VBE0

This register sets the Vertical Blank End count. It should be equal to the number of VIDCLKS in the vertical blank back porch plus the vertical sync period minus one.

NAME: VBLKGO
 ADDRESS: FSFF 6044
 ACCESS: READ/WRITE
 DEFAULT VALUE: 209 (HEX)

BIT 9	BIT 8	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
VBG9	VBG8	VBG7	VBG6	VBG5	VBG4	VBG3	VBG2	VBG1	VBG0

This register sets the Vertical Blank Start count. It should be equal to the number of VIDCLKS in the vertical blank back porch plus the vertical sync period plus the visible minus one.

NAME: VTOTAL
 ADDRESS: FSFF 6048
 ACCESS: READ/WRITE
 DEFAULT VALUE: 20C (HEX)

BIT 9	BIT 8	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
VT9	VT8	VT7	VT6	VT5	VT4	VT3	VT2	VT1	VT0

This register sets the Vertical Total count. It should be equal to the number of VIDCLKS in the total vertical period minus one.

NAME: HSYNCEND
 ADDRESS: FSFF 604C
 ACCESS: READ/WRITE
 DEFAULT VALUE: 00F (HEX)

BIT 9	BIT 8	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
X	HSE8	HSE7	HSE6	HSE5	HSE4	HSE3	HSE2	HSE1	HSE0

This register sets the Horizontal Sync End count. It should be equal to the number of VIDCLKS in the horizontal sync period minus one.

NAME: HBLKEND

ADDRESS: FSFF 6050

ACCESS: READ/WRITE

DEFAULT VALUE: 027 (HEX)

BIT 9	BIT 8	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
X	HBE8	HBE7	HBE6	HBE5	HBE4	HBE3	HBE2	HBE1	HBE0

This register sets the Horizontal Blank End count. It should be equal to the number of VIDCLKS in the horizontal blank back porch plus the horizontal sync period minus one.

NAME: HBLKGO

ADDRESS: FSFF 6054

ACCESS: READ/WRITE

DEFAULT VALUE: 0C7 (HEX)

BIT 9	BIT 8	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
X	HBG8	HBG7	HBG6	HBG5	HBG4	HBG3	HBG2	HBG1	HBG0

This register sets the Horizontal Blank Start count. It should be equal to the number of VIDCLKS in the horizontal blank back porch plus the horizontal sync period plus the visible period minus one.

NAME: HTOTAL

ADDRESS: FSFF 6058

ACCESS: READ/WRITE

DEFAULT VALUE: 0D7 (HEX)

BIT 9	BIT 8	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
X	HT8	HT7	HT6	HT5	HT4	HT3	HT2	HT1	HT0

This register sets the Horizontal Total count. It should be equal to the number of VIDCLKS in the total horizontal period minus one.

NAME: HHLFLIN
 ADDRESS: FSFF 605C
 ACCESS: READ/WRITE
 DEFAULT VALUE: 06B (HEX)

BIT 9	BIT 8	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
X	HH8	HH7	HH6	HH5	HH4	HH3	HH2	HH1	HH0

This register sets the Horizontal Half Line count for 30Hz mode. This register should be set to the number of visible pixels in X, divided by two, minus one

For more information on the NBSC chip refer to Appendix A.

4.3 Video Back End Chip (VBEC)

4.3.1 Introduction

The VBEC is a Toshiba ASIC of approximately 2,000 gates. It is designed to work in conjunction with the NBSC chip to control the video back end from the serial ports on the VRAM to the inputs of the DAC. It is capable of unpacking 1, 2, 4, and 8-bits per pixel data and feeding to the DAC with the proper input timing.

4.3.2 A look at the VBEC chip

The Video Back-end Chip (VBEC) is a 100 pin Rectangular Flatpac gate array implemented in 1.5 micron CMOS. It is part of a two chip set which comprise a frame buffer designed to connect to a NUBUS interface. The purpose of this chip is to interface the Video RAMs and Video timing generator to the DAC. It also takes the oscillator input and provides DACCLK and VIDCLK which is fixed at DACCLK / 4. This chip is designed to support a 640 X 480 pixel monitor and is capable of running up to 30.24 MHz. It was designed to interface to Brooktree parts BT478 or BT473. It is capable of running in five modes, 1 bit/pix , 2 bits/pix , 4bits/pix, 8bits/pix , and 24 bits/pix. In 24 bit mode , the VBEC takes 16 bits of red vram serial data , 16 bits of blue vram serial data and 16 bits of

green vram serial data. It takes the data for each channel, breaks it into two bytes and feeds it to the DAC at 2X the shift clock. In the other modes, only the data presented to the 16 bit red vram serial data input is used. These 16 bits are broken into 1, 2, 4 or 8 bit quantities and shifted out at 16X , 8X , 4X or 2x the shift clock. The outputs are replicated to the green and blue channels so all three channels fed to the DAC are identical.

For more information on the VBEC chip refer to Appendix B.

4.4 DAC

The Digital to Analog Converter is the BT473. The 473 has a palette of 16.7 million colors. Any access (byte, word, long) is allowed but the data must always be in 68020 byte lane 0 (data bits D31 - D24). For more information on DAC addressing and functions refer to the BT473 Data Sheets. ROM addresses lines A2, A1 and A0 are connected to BT473 pins RS2, RS1, and RS0 respectively and DACS(1:0) from the NBSC chip, are connected to BT473 pins S1 and S0 respectively. The addresses of the internal DAC registers are as follows:

Address Register RAM Write	FSFF 7000
Address Register RAM Read	FSFF 700C
Color LUT RAM	FSFF 7004
Pixel Read Mask Register	FSFF 7008
Address Register Overlay Write	FSFF 7010
Address Register Overlay Read	FSFF 701C
Overlay Register	FSFF 7014
Command Register	FSFF 7018

4.5 Configuration ROM

The Configuration ROM consists of two 27C64-250 EPROM IC physically wired to the 68020 byte lane 2 and 3 (data bits D31-D24). The Configuration ROM must have a value of 3C (hex) at location FsFF.FFFF. In addition other header information must be included in the Configuration ROM for the slot manager to function properly. See chapter 8 of the Macintosh II Specification for more details on this topic.

The Configuration ROM is 16-bits wide (two bytes), the data always appears in 68020 byte number 2 and 3 and any type of read access is allowed (byte, word, long).

The configuration ROM contains both a primary and secondary initialization, Apple compatible video driver, slot manager and video resources for 1, 2, 4, 8 and 24-bit mode, full chunky multiple resolution system. The primary initialization, when executed by the slot manager, initializes the DAC control registers, NBSC chip registers, and grays the screen.

4.5.1 Apple Board Identification

The 264 board is registered with Apple and has been assigned the following identifiers, which are reflected in the appropriate slot manager resources.

Board ID for ColorBoard 264 is \$xxxx.

Functional sResource ID for ColorBoard 264 is \$xxxx

4.5.2 Video Driver

The video driver supports open, close, control, and status calls. The open routine allocates private storage, stores a handle to private storage in the dCtlStorage field of the device control entry, initializes local variables, installs an interrupt handler, and enables VBL interrupts. The close routine disables VBL interrupts from the NBSC chip, removes the interrupt handler, and releases private storage. A list of supported driver calls follows.

Supported Video Driver Control Calls:

<u>csCode</u>	<u>Routine</u>
0	initialization
1	Kill I/O
2	SetMode
3	SetEntries
4	SetGamma
5	GrayScreen
6	SetGray
7	SetInterrupt

Supported Video Driver Status Calls:

<u>csCode</u>	<u>Routine</u>
0	Error
1	Error
2	GetMode
3	GetEntries
4	GetPages
5	GetBaseAddr
6	GetGray
7	GetInterrupt
8	GetGamma

5.0 Frame Buffer

The frame buffer is composed of three banks of Video RAM (VRAM). It is organized as a red bank 1024 x 512 x 8, and similar green and blue banks. The green and blue banks are active only in 24-bit mode.

APPENDIX A - NUBUS SYSTEM CONTROLLER INFORMATION

A.1 Pin Descriptions

- NUBUS INTERFACE -

SLOTID 3:0	These pins provide the slot id to the NBSC chip from the NUBUS card.
NUBUSD 31:0	These pins provide a buffered version of the NUBUS AD bus to the NBSC chip .
BUSCLK	This is a buffered version of the NUBUS clock which provides the primary clock to the NBSC chip.
B15CLK	This is a 24 ns delayed version of the buffered NUBUS clock. Internally it is used to switch the VRAM address from the row address value to the colum address value.
B30CLK	This is a 36 ns delayed version of the buffered NUBUS clock. Internally it is used to shape the CAS* signal.
+START	This is an inverted version of the NUBUS /START signal.
+NBACK	This is an inverted version of the NUBUS /ACK signal.
+NBTM1	This is an inverted version of the NUBUS /TM1 signal.
+NBTM0	This is an inverted version of the NUBUS /TM0 signal.
-RESET	This is a buffered version of the NUBUS /RESET signal and is used to reset the NBSC chip.
NBIN-	This is the direction control line for the bidirectional NUBUS data buffers.

NCBIN-	This is the direction control line for the bidirectional NUBUS control line buffers.
NMRQ	This signal is the vertical count = 0 interrupt. This signal is inverted then drives the NUBUS /NMRQ line.

- ROM and DAC INTERFACE -

-ROMOE	This signal is used to chip enable and output enable the system ROM.
ROMADDR 12:0	These address lines are latched from the NUBUS address bus when a ROM or a DAC access is made. The twelve lines are connected to the ROM and ROMADDR 2:0 are connected to the DAC signals RS 2:0.
DACS 1:0	These are general purpose status register outputs which are used to control the DAC signals S1 and S0.
-DACRD	This line drives the DAC's read line.
-DACWR	This line drives the DAC's write line.

- VIDEO INTERFACE -

-EXHSYN	This is the input for the external horizontal sync signal. This input triggers a one shot at the first detected falling edge.
-EXVSYN	This is the input for the external vertical sync signal. This input triggers a one shot at the first detected falling edge.
-EXSYNP	This is the input for the external composite sync signal. This input triggers a one shot at the first detected falling edge.
VIDCLK	This is the clock for the video timing generation circuits in NBSC chip.
CBLANK	This is the active high composite blank signal which goes to VBEC.

CSYNC	This is the active high composite sync signal which goes to VBEC.
CHUNKY	This is one of the VBEC mode control signals.
MODE1	This is one of the VBEC mode control signals.
MODE0	This is one of the VBEC mode control signals.
OSCSEL	This is the oscillator select control line which goes to VBEC.

- BOARD STATUS INPUTS -

OPTON	This signal is pulled down when the VRAM option board is plugged in. It can be read in a status register.
MTYPE	This line may be pulled up or down depending on the monitor which the board is connected to. It can be read in a status register.
MPRES	This is a general purpose input intended to have a monitor detecting circuit attached.

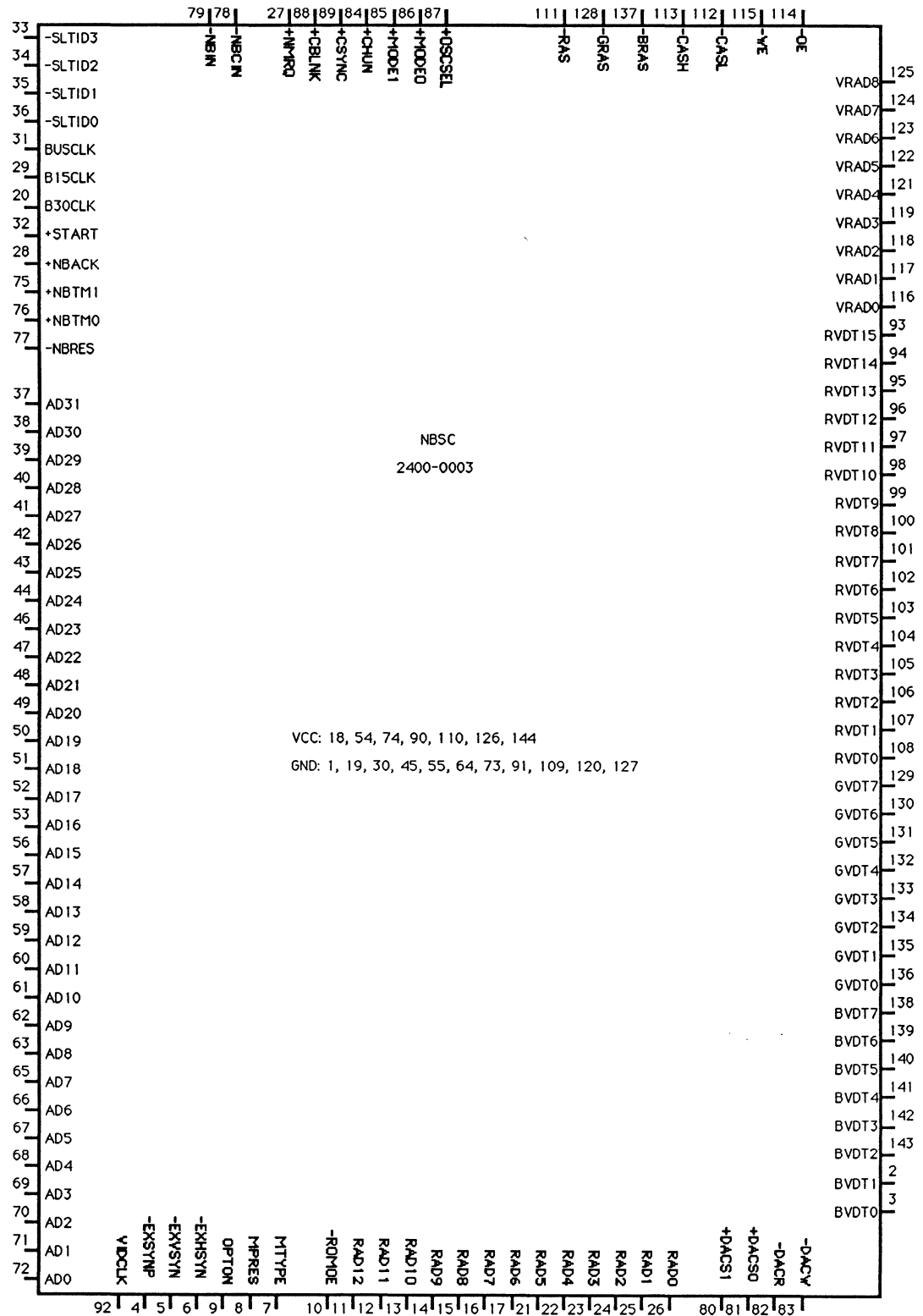
- VIDEO RAM INTERFACE -

-RRAS	This is the VRAM -RAS signal used for the Red VRAM bank.
-GRAS	This is the VRAM -RAS signal used for the Green VRAM bank.
-BRAS	This is the VRAM -RAS signal used for the Blue VRAM bank.
-CASH	This is the VRAM -CASH signal.
-CASL	This is the VRAM -CASL signal.
-WE	This signal is the VRAM -WE signal.
-OE	This signal is the VRAM -OE signal.
VRAD 8:0	These are the VRAM address signals.

REDRD 15:0	This is the data bus for the Red bank of VRAMs. Typical connection is shown in the 264 schematics.
GREENRD7:0	This is the data bus for the Green bank of VRAMs. Typical connection is shown in the 264 schematics.
BLUERD 15:0	This is the data bus for the Blue bank of VRAMs. Typical connection is shown in the 264 schematics.

A.3 Pinout

On next page.



A.3 Electrical Information

Inputs

Vil	.8V
Vih	2.0v
Iil	+10uA
Iih	10uA

Outputs

-RRAS , -GRAS , -BRAS , -CASH , -CASL and VRAD 8:0

Vol	.6V
Voh	4.0v
Ioh	6ma
Iol	-6mA

All other outputs

Vol	.6V
Voh	4.0v
Ioh	4ma
Iol	-4mA

Load

Max capacitance	80pf for -CASH , -CASL and VRAD 8:0
Max capacitance	50pf for -RRAS , -GRAS and -BRAS

All other outputs

Max capacitance	40pf for any output except -WE and -OE
Max capacitance	90pf for -WE and -OE

A.4 Timing Information (All times in nS unless otherwise specified)

- NUBUS INTERFACE -Inputs

SLTID 3:0 , START, NBACK , NBTM 1:0 , -RESET , NUBUSD 31:0

14ns setup and 1ns hold relative to BUSCLK.

Outputs

-NBCIN , -NBIN , NMRQ , NBTM 1:0 , NBACK

BUSCLK to out	min 3	max 22
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NUBUSD 31:0

BUSCLK to out	min 4	max 28
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Clocks

BUSCLK - this is a 10MHz max clock with a 30% - 70% duty cycle.

B15CLK - this is a delayed version of BUSCLK. The delay is 24 +-2 nsec.

B30CLK - this is a delayed version of BUSCLK. The delay is 36 +-2 nsec.

- ROM and DAC Interface -DAC

Address setup to -RD or -WR	180 min
Address hold to -RD or -WR	200 min
-WE pulse width	80 min
Data Setup to -WR	100 min
Data Hold to -WR	200 min
-RD to data valid	80 max

ROM

Address access	370 max
-OE , -CE access	270 max

- VIDEO INTERFACE -

-EXHSYN , -EXVSYN , -EXSYNP

These signals require 8 setup and 10 hold relative to the falling edge of VIDCLK.

VIDCLK - This clock is PixClk/4. It must have a 40%-60% duty cycle.

CBLANK, CSYNC, CHUNKY , MODE1 , MODE0 and OSCSEL

These outputs have clock to out of 18 max , 2 min relative to VIDCLK.

- BOARD STATUS INPUTS -

OPTON , MTYPE , MPRES

These are designed to be static in normal operation. They have a three level register to register synchronization. They have 10 ns setup and 10 ns hold relative to BUSCLK if they are to perform synchronously.

- VIDEO RAM INTERFACE -

The VRAM signal will all be listed as CLK to Lo and CLK to Hi.

-RRAS, -GRAS , -BRAS

Rising	18.2 max	5.1 min	(relative to BUSCLK rising)
Falling	16.2 max	4.6 min	(relative to BUSCLK rising)

-CASH , -CASL

Rising	24.2 max	6.6 min	(relative to BUSCLK rising)
Falling	20.5 max	5.7 min	(relative to B30CLK rising)

-WE , -OE

Rising	19.8 max	5.6 min	(relative to B30CLK rising)
Falling	25.5 max	5.7 min	(relative to B30CLK rising)

VRAD

Row Add	7.2 max	-2.2 min	(relative to BUSCLK rising)
Col ADD	23.9 max	6.5 min	(relative to B15CLK rising)

REDRD , GREENRD , BLUERD

Wr Val	20.6 max	5.8 min
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Read Data setup time is relative to CAS. The VRAM max CAS to Data delay is 50 ns. Read Data hold time is relative to CAS. The VRAM must provide 5 ns Hold

A.5 Performance

- 1, 2, 4, and 8-Bit Mode

Normal Read/Write	400 nS/32-bit word
Block Mode, Block Size = 2	600 nS/2 32-bit words
Block Mode, Block Size = 4	1000 nS/4 32-bit words
Block Mode, Block Size = 8	1800 nS/4 32-bit words
Block Mode, Block Size = 16	3400 nS/4 32-bit words

- 24-Bit Mode (Full Chunky)

Normal Read/Write	300 nS/32-bit word
Block Mode, Block Size = 2	400 nS/2 32-bit words
Block Mode, Block Size = 4	600 nS/4 32-bit words
Block Mode, Block Size = 8	1000 nS/4 32-bit words
Block Mode, Block Size = 16	1800 nS/4 32-bit words

A.6 Known Bugs in the NBSC

- 1 - The -OE signal extends beyond -RAS during transfer cycles.
Fix - A transfer cycle is detected and -OE is truncated with the falling edge of RAS
- 2 - In 1, 2, 4, and 8-bit mode write data is word swapped.
Fix - A0 must be inverted in 1, 2, 4, and 8-bit mode.
- 3 - In Chunky mode CASH and CASL are swapped.
Fix - CASH and CASL are switched to the Blue and Green memory bank and the red serial data is byte swapped with a multiplexer to the VBEC chip

APPENDIX B - VIDEO BACK END INFORMATION

B.1 Pin Descriptions

INPUTS

OscSel , Ocs1 , Os0

The VBEC provides for two oscillator inputs , Osc1 and Ocs0. OscSel selects which of the two inputs is used to generate DACCLK and VIDCLK according to the following table.

OscSel	Input
0	OscSel0
1	OscSel1

Chunky , Mode1 , Mode0

These bits are used to determine which of the five possible modes the VBEC operates in according to the following table.

Chunky	Mode0	Mode1	Operating Mode
1	1	1	24 bits/pix
1	0	*	Reset Mode
1	*	0	Reset Mode
0	1	1	8 bits/pix
0	1	0	4 bits/pix
0	0	1	2 bits/pix
0	0	0	1 bit/pix

-Note: Reset Mode is a function built in for ASIC testability requirements. When the chip is in this mode the circuit which generates VIDCLK is reset and VIDCLK is held low. This mode is forbidden in operation.

CBLANK CBLANK is the active high composite blank input. This input should be synchronous to VIDCLK. It is latched on the rising edge of VIDCLK , inverted and delayed 5 additional PIXCLKs then presented to the DAC. This delay allows VBEC to produce the shift clocks to the VRAMs and synchronize the video data with -DACBL going to the DAC.

- CSYNC** CSYNC is the active high composite sync input. This input should be synchronous to VIDCLK. It is latched on the rising edge of VIDCLK, inverted and delayed 5 additional PIXCLKs then presented to the DAC. This delay is provided to match the CBLANK delay.
- RSD(15:0)** RSD[15:0] is the input for the serial data from the Red Bank of video rams. In 24 bit mode it is used for the Red channels video data. In the other 4 modes it is the only channel used for serial data and the produced output is duplicated on all three data channels to the DAC.
- BSD(15:0)** BSD[15:0] is the input for the serial data from the Blue Bank of video rams. In 24 bit mode it is used for the Blue channels video data. In the other 4 modes it is ignored.
- GSD(15:0)** GSD[15:0] is the input for the serial data from the Green Bank of video rams. In 2-bit mode it is used for the Green channels video data. In the other 4 modes it is ignored.

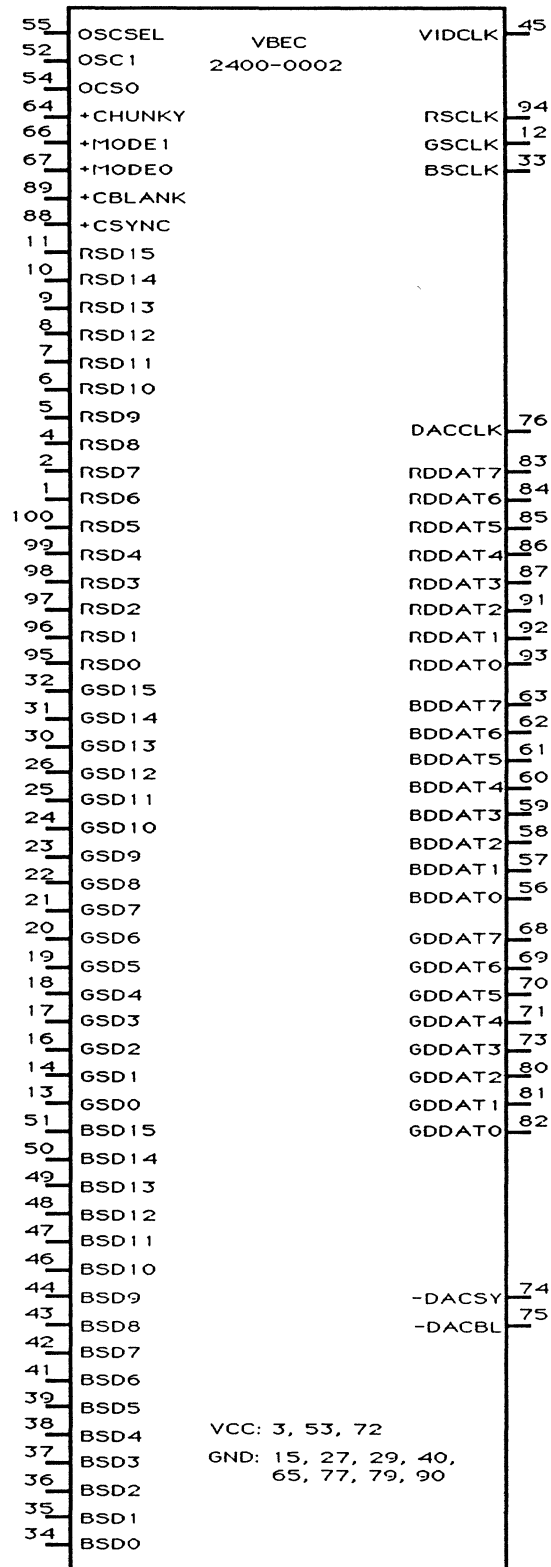
OUTPUTS

- DACBL** -DACBL is the active low composite blank signal for the DAC. It is an inverted and delayed version of the CBLANK input. This delay allows VBEC to produce the shift clocks to the VRAMs and synchronize the video data with -DACBL going to the DAC.
- DACS** -DACS is the active low composite sync signal for the DAC. It is an inverted and delayed version of the CSYNC input. This delay is provided to match the CBLANK delay.
- DACCLK** DACCLK is the clock provided for the DAC. It is a propagation delayed version of the selected oscillator input.
- VIDCLK** VIDCLK is a 50% duty cycle clock with a frequency of one forth the selected oscillator input.
- RSCLK** RSCLK is the shift clock provided to the Red Bank of video rams. It is synchronized to blank to provide valid video data to the DAC synchronous to -DACBL. RSCL is active in all operating modes.

GSCLK	GSCLK is the shift clock provided to the Green Bank of video rams. It is synchronized to blank to provide valid video data to the DAC synchronous to -DACBL. GSCLK is active only in 24 bit mode.
BSCLK	BSCLK is the shift clock provided to the Blue Bank of video rams. It is synchronized to blank to provide valid video data to the DAC synchronous to -DACBL. BSCLK is active only in 24 bit mode.
RDDAT(7:0)	RDDAT[7:0] is the video data provided to the DACs Red Channel.
GDDAT(7:0)	GDDAT[7:0] is the video data provide to the DACs Green Channel.
BDDAT(7:0)	BDDAT[7:0] is the video data provide to the DACs Blue Channel.

B.2 Pinout

On next page.



B.2 Electrical Information

Inputs

Vil	.8V
Vih	2.0v
Iil	+10uA
Iih	10uA

Outputs

Vol	.6V
Voh	4.5v
Ioh	4ma
Iol	-4mA

Max capacitance 40pf for any output

B.3 Timing Information

Ocs1 , Osc0

The oscillator inputs are allowed to be frequencies of up to 30.24MHz and must have a 50% +/-10% duty cycle.

OcsSel

This signal is assumed to be stable at least 12 clocks before the end of reset and not change in normal operation. If It is changed, results are unpredictable but video should stabilize after one frame time.

CBlank , CSync , Chunky , Mode0 , Mode1

These signals are only allowed to change during vertical blank. If they change at any other time video may be garbage for up to one frame time.

RSD

Red serial data timing assumes you are using RSCLK as the shift clock to the rams. Relative RSCLK access time tSCA max = 30ns and hold time tSOH=5ns.

BSD

Blue serial data timing assumes you are using BSCLK as the shift clock to the vide rams. Relative BSCLK access time $t_{SCA} \max = 30\text{ns}$ and hold time $t_{SOH} = 5\text{ns}$.

GSD

Green serial data timing assumes you are using GSCLK as the shift clock to the vide rams. Relative GSCLK access time $t_{SCA} \max = 30\text{ns}$ and hold time $t_{SOH} = 5\text{ns}$.

-DACBL , -DACSY , BDDAT , GDDAT , RDDAT

The timing of these signals is all relative to DACCLK. Each of these signals is guaranteed to have 6ns setup and 6 ns hold relative to DACCLK.

VIDCLK , DACCLK , RSCLK , BSCLK , GSCLK

These clocks are derived from the selected oscillator input and their relationships are described below.

OSC rising to DACCLK rising	max 12ns	min 2ns
OSC falling to DACCLK falling	max 17ns	min 2.5ns
OSC rising to VIDCLK rising	max 28ns	min 4ns
OSC rising to VIDCLK falling	max 32ns	min 5ns
OCS rising to RSCLK rising	max 29ns	min 4ns
OSC rising to RSCLK falling	max 33ns	min 5ns
OCS rising to GSCLK rising	max 30ns	min 4ns
OSC rising to GSCLK falling	max 34ns	min 5ns
OCS rising to BSCLK rising	max 30ns	min 4ns
OSC rising to BSCLK falling	max 34ns	min 5ns